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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,868	11/15/2001	Michael Belman	P05378US0	4795
22885	7590	04/15/2003		
MCKEE, VOORHEES & SEASE, P.L.C. 801 GRAND AVENUE SUITE 3200 DES MOINES, IA 50309-2721			EXAMINER	
			SEFER, AHMED N	
			ART UNIT	PAPER NUMBER
			2826	
DATE MAILED: 04/15/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

A2

Office Action Summary	Application No.	Applicant(s)	
	10/002,868	BELMAN, MICHAEL	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 February 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 and 8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-4 and 8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>7</u> .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/4/03 has been entered and claims 5-7 have been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al. US Patent No. 6,404,324 in view of admitted prior art (APA).

Witt et al disclose in figs. 1-5 a chip resistor 10 comprising a substrate 12 having opposite parallel symmetrical top and bottom surfaces, and a central longitudinal plane of symmetry; separate and spaced first and second resistive layers 14, 16 on the top and bottom surfaces, respectively, electrically connected in parallel to each other and the top and the bottom surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof; wherein an area of the first resistive layer is substantially equal to that of the second resistive layer such that the chip resistor with both resistive layers tolerates higher instantaneous pulsed power than either layer could provide separately and individually; and first and second terminals for surface

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mounting, each terminal being electrically connected to the first and second resistive layers, but do not disclose the terminals being symmetrical about a central longitudinal plane.

APA discloses in fig. 1 terminal 16 being substantially symmetrical about a central longitudinal plane.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the terminals of the APA with the device of Witt et al, since that would facilitate input/output areas.

As to claim 8, Witt et al disclose first resistive layer and second resistive layer are symmetric about the central longitudinal plane.

4. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al. US Patent No. 6,404,324 in view Uehara (JP 5-90003).

Witt et al disclose in figs. 1-5 a chip resistor 10 comprising a substrate 12 having opposite parallel symmetrical top and bottom surfaces, and a central longitudinal plane of symmetry; separate and spaced first and second resistive layers 14, 16 on the top and bottom surfaces, respectively, electrically connected in parallel to each other and the top and the bottom surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof; wherein an area of the first resistive layer is substantially equal to that of the second resistive layer such that the chip resistor with both resistive layers tolerates higher instantaneous pulsed power than either layer could provide separately and individually; and first and second terminals for surface

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mounting, each terminal being electrically connected to the first and second resistive layers, but do not disclose the terminals being symmetrical about a central longitudinal plane.

Uehara discloses in figs. 1 and 2 a chip resistor comprising terminals 5/5a and electrically connected to thick resistors 2, 2a (as in claim 2) and being substantially symmetrical about a central longitudinal plane.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Uehara with the device of Witt et al, since that would facilitate input/output areas.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al in view of Uehara as applied to claim 1 above, and further in view of Huck US Patent No. 5,543,775.

The combined references disclose the device structure as recited in claim 1, but do not specifically teach the use of thin film resistive layers.

Huck teaches (see abstract) the advantage of using thin film resistive layers in temperature sensing devices or as a resistance heating element.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ a thin film resistive layer, since thin film resistive layers would react more quickly to a surge.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Witt et al in view of Uehara as applied to claim 1 above, and further in view of Thompson US Patent No. 4,064,477.

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The combined references disclose the device structure as recited in claim 1, but do not specifically teach the use of foil resistive layers.

Thompson discloses (see col. 1, lines 5-26) a foil resistive layer.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to substitute the thin or thick film resistive layer of the prior art with a foil resistive layer, since that would allow a uniform current density.

Response to Arguments

7. Applicant's arguments with respect to claim 1 has been considered but are not persuasive. The recitation "a pick-and-place machine" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Szwarc et al. US ref. 5,999,085 disclose a surface mounted four terminal resistor capable of handling short pulses of high power.

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9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
April 7, 2003


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800